AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

Claim 1. (Previously Presented) A system comprising:

no more than one arithmetic logic unit operating in split mode to determine trace bits for Viterbi decoding of a binary convolution code;

a first register and a second register, both coupled to said arithmetic logic unit, to jointly store at most a single copy of said trace bits.

Claim 2. (Previously Presented) A system according to claim 1 wherein said first register is to store a first half of a series of trace bits for states of said code in sequential order and said second register is to store a second half of said series in sequential order.

Claim 3. (Previously Presented) A system according to claim 2 wherein said first half comprises trace bits for a first half of said states and said second half comprises trace bits for a second half of said states.

Claims 4 – 5. (Cancelled)

Claim 6. (Original) A system according to claim 1 and wherein said first register and said second register are shift registers.

Claim 7. (Previously Presented) A system according to claim 1, the system further comprising:

a first barrel shifter between said first register and said arithmetic logic unit and a second barrel shifter between said second register and said arithmetic logic unit.

Claim 8. (Currently Amended) A system comprising:

a storage device having at least three memory cell groups for storing in sequential order trace bits of at least three stages of Viterbi decoding of a binary convolution code, such that the trace bits of said at least three stages are simultaneously maintained by said storage device.

wherein each of said memory cell groups includes at least one memory cell for storing in sequential order trace bits of one of said stages.

~~a storage device having memory cells, wherein a group of at least one memory cell is to store all trace bits for a stages of Viterbi decoding of a binary convolution code in sequential order, another group of at least one memory cell is to store all trace bits for a subsequent stage of Viterbi decoding of said binary convolution code in sequential order, and yet another group of at least one memory cell is to store all trace bits for a further subsequent stage of Viterbi decoding of said binary convolution code in sequential order~~.

Claim 9. (Cancelled)

Claim 10. (Currently amended) A system according to claim 8 and wherein at least one of said memory cell groups ~~group~~ consists of one memory cell.

Claim 11. (Cancelled)

Claim 12. (Currently amended) ~~A system comprising:~~

The a ~~storage device~~ system of claim 8, ~~having groups of memory cells,~~ wherein the number of memory cells in each of said memory cell groups is a power of 2 and is at least 2, ~~said memory cells to store trace bits for Viterbi decoding of a binary convolution code in sequential order, and wherein in each of said groups, a first half of said memory cells are to~~

~~jointly store a first half of a series of trace bits for three or more states of said code and a second half of said memory cells are to jointly store said second half of said series.~~

Claim 13 – 18. (Cancelled)

Claim 19. (Previously Presented) A binary convolution decoder having multiple stages, each stage having states of a binary convolution code, the decoder comprising:

at least one arithmetic logic unit to determine trace bits for each of said states for each of said multiple stages;

a first register and a second register to jointly store a single copy of trace bits of at least a portion of one stage;

a storage device having memory cells, wherein for each of said multiple stages, a group of one or more memory cells is to store said trace bits in sequential order; and

means for tracing back, stage by stage, through said memory cells using said trace bits.

Claim 20. (Previously Presented) A decoder according to claim 19, wherein said means for tracing back is to trace back in as few as two clock cycles per stage.

Claim 21. (Previously Presented) A decoder according to claim 19, wherein each of said stages has 16 states, each of said memory cells has a length of at least 16 bits and said means for tracing back is to trace back in as few as two clock cycles per stage.

Claim 22. (Previously Presented) A decoder according to claim 19, wherein each of said stages has 32 states, each of said memory cells has a length of at least 32 bits and said means for tracing back is to trace back in as few as two clock cycles per stage.

Claim 23. (Previously Presented) A decoder according to claim 19, the decoder further comprising:

a trace back register whose L+P-1 least significant bits indicate the location in said group of a bit whose trace bit is to be saved into the least significant bit of the trace back register after the trace back register is shifted right one bit, said location comprising the bit number given by the L least significant bits of the trace back register and the memory cell whose number in said group is given by the value in the P-1 bits of the trace back register immediately to the left of said L least significant bits, where L is the integer part of the logarithm to base 2 of the length of the memory cell and P is the number of memory cells in said group.

Claims 24 – 26. (Cancelled)

Claim 27. (Currently amended) A method comprising:

generating a series of trace bits for Viterbi decoding of a binary convolution code;

storing a first half of said series sequentially in a first register and a second half of said series sequentially in a second register; and

saving ~~said trace bits~~ in sequential order the trace bits stored in said first and second registers to a group of one or more memory cells.

Claim 28. (Previously Presented) A method according to claim 27, wherein said first half comprises trace bits for a first half of states of said code and said second half comprises trace bits for a second half of said states.

Claim 29. (Cancelled)

Claim 30. (Previously Presented) A method according to claim 27, wherein said group consists of one memory cell.

Claim 31. (Cancelled)

Claim 32. (Previously Presented) A method according to claim 27, the method further comprising:

storing said trace bits in sequential order in groups of memory cells, wherein the number of memory cells in each of said groups is a power of 2 and at least 2,

wherein in each of said groups, a first half of said memory cells jointly store said first half of said series of trace bits and a second half of said memory cells jointly store said second half of said series.

Claim 33 – 38. (Cancelled)

Claim 39. (Currently amended) A method for Viterbi decoding of binary convolution codes, the decoding involving multiple stages each having states of a binary convolution code, the method comprising:

determining trace bits for each of said states for each of said multiple stages;

storing a single copy of trace bits of at least a portion of one stage jointly in a first register and a second register;

for each of said multiple stages, storing said trace bits in sequential order in a group of one or more memory cells of a storage device such that the trace bits of at least three of said stages are simultaneously maintained by said storage device; and

tracing back, stage by stage, through said memory cells using said trace bits.

Claim 40. (Previously Presented) A method according to claim 39, wherein tracing back through said memory cells is performed in as few as two clock cycles per stage.

Claim 41. (Previously Presented) A method according to claim 39, wherein each of said stages has 16 states, each of said memory cells has a length of at least 16 bits and tracing back through said memory cells is performed in as few as two clock cycles per stage.

Claim 42. (Previously Presented) A method according to claim 39, wherein each of said stages has 32 states, each of said memory cells has a length of at least 32 bits and tracing back through said memory cells is performed in as few as two clock cycles per stage.

Claim 43. (Previously Presented) A method according to claim 39, wherein tracing back through said memory cells comprises for each stage:

shifting a trace back register left one bit;

saving into the least significant bit of said trace back register the trace bit located in the memory cell whose number in said group is given by the value of the P-1 bits of said trace back register immediately to the left of the L least significant bits of said trace back register and located at the bit number given by said L least significant bits of said trace back register, where L is the integer part of the logarithm to base 2 of the length of the memory cell and P is the number of memory cells in said group.

Claim 44. (Currently amended) A method comprising:

tracing back, stage by stage, in as few as two clock cycles per stage, states of binary convolution codes that are decoded using Viterbi decoding, based on sequentially stored trace bits of two or more of said stages.

Claim 45. (Previously Presented) A method according to claim 44, wherein tracing back said states comprises:

in a first clock cycle, generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state, and identifying a trace bit of a state of a previous stage, where an index of said state of said previous stage is given by said generated B-bit binary representation; and

in a second clock cycle, storing said trace bit of said state of said previous stage in a single bit of temporary storage,

wherein B is the logarithm to base 2 of the number of states in a stage.

Claim 46. (Previously Presented) A method according to claim 45, wherein generating said generated B-bit binary representation comprises:

multiplying B bits of a memory element by two to produce a product;

adding the content of said single bit of temporary storage to said product to produce a sum; and

storing the B least significant bits of said sum in said B bits of said memory element.

Claim 47. (Previously Presented) A method according to claim 45, further comprising:

storing trace bits for states of a stage in a single memory cell having a length of at least the number of states in a stage,

wherein identifying said trace bit of said state of said previous stage comprises generating from said generated B-bit binary representation an address of a bit of said single memory cell that comprises said trace bit of said state of said previous stage.

Claim 48. (Previously Presented) A method according to claim 47, wherein said trace bits are stored sequentially in said single memory cell and said address is said index of said state of said previous stage.

Claim 49. (Previously Presented) A method according to claim 46, further comprising:

storing trace bits for states of a stage in two or more memory cells having a total number of bits at least the number of states in a stage,

wherein identifying said trace bit of said state of said previous stage comprises generating from said generated B-bit binary representation an address of a bit of said memory cells that comprises said trace bit of said state of said previous stage.

Claim 50. (Previously Presented) A method according to claim 49, wherein generating said address comprises:

addressing a particular memory cell by the content of the (P-1) most significant bits of said B bits of said memory element; and

addressing a particular bit in said particular memory cell by the content of the L least significant bits of said B bits of said memory element,

wherein L is the integer part of the logarithm to base 2 of the number of states stored in each of said memory cells, and P is the number of said memory cells.

Claim 51. (Previously Presented) A method to be used in Viterbi decoding of binary convolution codes, the decoding involving multiple stages each having states of a binary convolution code, the method comprising:

generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state; and

identifying a trace bit of a state of a previous stage, where an index of said state of said previous stage is given by said generated B-bit binary representation,

wherein B is the logarithm to base 2 of the number of states in a stage.

Claim 52. (Previously Presented) A method according to claim 51, further comprising:

storing said trace bit of said state of said previous stage in a single bit of temporary storage.

Claim 53. (Previously Presented) A method according to claim 52, wherein generating said B-bit binary representation comprises:

multiplying B bits of a memory element by two to produce a product;

adding the content of said single bit of temporary storage to said product to produce a sum; and

storing the B least significant bits of said sum in said B bits of said memory element.

Claim 54. (Previously Presented) A system to perform tracing back, stage by stage, in as few as two clock cycles per stage, states of binary convolution codes that are decoded using Viterbi decoding, the system comprising:

temporary storage having a single bit to store a trace bit; and

a memory element to store in its B least significant bits a B-bit binary representation of an index of a state of a stage, where B is the logarithm to base 2 of the number of said states.